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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/661,019	09/12/2003	Feng Chen	TI-35765 (032350.B523)	6817	
23494	7590 02/24/2005		EXAM	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999			JEAN PIERRE, PEGUY		
DALLAS, TX			ART UNIT PAPER NUMBER		
			2819		
			DATE MAILED: 02/24/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	•			
Office Action Summary		10/661,019	CHEN, FENG				
		Examiner	Art Unit				
		Peguy JeanPierre	2819				
The MAILING DA	ATE of this communication app	ears on the cover sheet with the c	orrespondence ad	dress			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1) Responsive to co	ommunication(s) filed on 18 Ja	nuary 2005.					
2a) This action is FIN	·						
closed in accorda	ance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	63 O.G. 213.				
Disposition of Claims							
4a) Of the above 5)⊠ Claim(s) <u>13-18 a</u> 6)⊠ Claim(s) <u>1,2,7,8</u> 7)⊠ Claim(s) <u>3-6 and</u>		vn from consideration.					
Application Papers							
 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on 9/12/2003 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. 							
Priority under 35 U.S.C. §	i 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
Attachment(s)							
	atent Drawing Review (PTO-948) tement(s) (PTO-1449 or PTO/SB/08)	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ate	D-152)			

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-2, 7-8, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Connell et al. (USP 5,940,447) or Khoury et al. (USP 6,121,910).

Connell et al. disclose in Figure 1, a method for digitizing a signal that comprises a sample and hold circuit (36) that samples an analog input signal having a particular frequency, a filter (38) that filters the sampled signal, a quantizer/comparator (40) that quantizes the filtered signal to generate the digital signal representing the information that is contained in the analog input signal. The filter is a passive bandpass or highpass filter circuit (see col. 3,lines 31-32) that comprises at least one passive element such as a switched capacitor circuit (see col. 4 lines 1-2).

Khoury et al. disclose in Figure 1, a sigma delta modulator to digitize an analog input signal having an intermediate frequency signal (fin). The converter comprises a filter (104) that can be implemented as a bandpass or highpass filter (see col. 4, lines 48-53), a quantizer (108) that can be implemented as a comparator or ADC converter (see col. 4, lines 65-67).

Allowable Subject Matter

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3. Claims 3-6 and 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 13-18 and 20 allowed.

Response to Arguments

- 5. Applicant's arguments, see remarks, filed 1/18/2005, with respect to claims 3-4 and 8-10 have been fully considered and are persuasive. The rejection of claims 3-4 and 8-10 has been withdrawn.
- 6. Applicant's arguments filed on 1/18/2005 have been fully considered but they are not persuasive. Applicant argues that claim 1 recites the step of "... sampling an analog signal..." Applicant further argues that the signal in the Connell reference is not apparently an analog signal. The Examiner disagrees. Figure 2 of the Connell shows a sample and hold (SH) circuit that is represented by capacitors (216, 218). The sample and hold circuit is coupled to analog input signal (IN+, IN-). Apparently, the input signal represents the coil signal (20). There is no indication in the reference that the input signal to the sample and hold circuit is binary or any digital data signal. Absence of such a recitation, the Examiner regards the signal inputted to the sample and hold as an analog signal. It is to be noted that block 34 of Figure 1 is designed to process analog signal. As set forth in the rejection, the sampled output signal is inputted into a bandpass filter. Inherently, the output of the filter is a filtered signal; in addition, because the filter is a bandpass filter it is inherent that it provides a bandpass response. Applicant further argues that the filter circuit comprises at least one passive element.

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The Connell reference describes a filter formed of switched capacitor circuit that is known in the art as passive element circuit. See rejection. In addition, a comparator is regarded as a quantizer because both circuit elements can be implemented to convert analog signal to digital data. In fact, the specification describes the quantizer (16) as a

high speed comparator.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peguy JeanPierre whose telephone number is (571)

272-1803272-1803. The examiner fax phone number is (571) 273-1803.

Peguy JeanPierre Primary Examiner PEGUY JEANPIERRE PRIMARY EXAMINER